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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,082	09/08/2003	MIN-LUNG HUANG	10228-US-PA	2081

31561 7590 06/08/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
TSAI, H JEY	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,082	HUANG ET AL.	
	Examiner	Art Unit	
	H.Jey Tsai	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9 and 11-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9 and 11-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 12-13 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ratificar et al. 2003/0121958 in view of Kunimatsu et al. 5,767,564 and Nguyen et al. 6,238,949, all are previously cited.

The reference(s) teach the features:

a die 100 having an active surface and a back surface wherein the active surface is implemented with a plurality of bonding pads 110, fig. 1a and para. 14+,

an under-bump-metallurgy layer 130 disposed over the bonding pads 110, para. 17,

a patterned dielectric layer 120 over the active surface of the die, wherein the patterned dielectric layer 120 has a plurality of openings 125 that expose the bonding pads 110 and the UBM layer is disposed above the patterned dielectric layer, fig. 1b,

a plurality of solder blocks 150, respectively disposed above the under-bump metallurgy layer 130,

a passive component 170 (a substrate that includes passive electronic components, para. 13) having a plurality of terminal electrodes, para. 26,

the terminal electrodes 160/172 are respectively coupled to the UBM layer through the solder blocks 150/155.

Kunimatsu et al. substantially discloses a chip structure and a chip package structure, which includes :

a substrate 1 (called package) having an upper surface, fig. 1+ and col. 3, lines 34+,

a die 2 (called semiconductor element) having an active surface and a back surface, wherein the back surface of the die 2 is in contact with the upper surface of the substrate 1 (called package) and the active surface is implemented with a plurality of bonding pads, see fig. 2-3, and col. 4, lines 13+,

a solder block 3A disposed on the die 2, figs. 2-3 and col. 4, lines 32+,

a passive component 3 (a capacitor) with a plurality of terminal electrodes 5, 7, 8 wherein the terminal electrodes are coupled to the solder block 3A, col. 4, lines 38+,

a plurality of conductive wires electrically connecting the die 2 and the substrate 1.

Nguyen et al. teaches at col. 1, lines 15-22, col. 3, lines 34-38 using a plastic as an encapsulant for a chip package.

The difference between the reference(s) and the claims are as follows: Ratifiecar et al. teaches mounting a substrate that can be a passive component of capacitor to a die through a UBM layer to the solder block but does not teach that at least two terminal electrodes are respectively disposed at two ends of the passive component and using plastic to encapsulate the die. However, Kunimatsu et al. teaches at figs. 1-5, two

terminal electrodes 3A are respectively disposed at two ends of the passive component 3. And, Nguyen et al. teaches at col. 1, lines 15-22, col. 3, lines 34-38 using a plastic as encapsulant to form a packaged integrated circuit.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Ratificar et al.'s process with two terminal electrodes are respectively disposed at two ends of the passive component as suggested by Kunimatsu et al. because there must have two terminal electrodes as input and output terminals of a passive electronic component to be functional and using a plastic package as suggested by Nguyen et al. because plastic package is less expensive than other type of chip package.

Claims 11 and 14 are rejected under 35 U.S.C 103 as being unpatentable over Ratificar et al. in view of Kunimatsu et al. and Nguyen et al. as applied to claims 9, 12-13 and 15-16 above, and further in view of Lin 6,303,423.

The difference between the references applied above and the instant claim(s) is: Primary reference Ratificar et al. in view of Kunimatsu et al. and Nguyen et al. does not teach a re-distribution layer is connected to the bond pad. However, Lin '423 teach at col. 7, lines 37-53 and figure 4 and 11 that a network of electrical connections formed from conductive line 13 is connected to bonding pad 16.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings with a re-distribution layer as taught by Lin '423 because passive component formed over the die can be re-distribute to the circuit formed in the die.

Conclusion

Applicant's arguments filed April 22, 2005 have been fully considered but they are not persuasive. Ratificar et al. clearly teaches at para. 13 and fig. 2a, substrate 170 can be a passive component, such as resistor or capacitor etc. having terminal electrodes coupled to the UBM layer through solder blocks 160/155. Since. substrate is bonded to the 1/0 pads, of die, hence, it is clearly that substrate which is a passive component must have at least two terminals corresponding to the 1/0 pads of the die (one to input pad and the other to output pad). And. it is not only obvious but also inherent that a passive component must have at least two terminals to receive electric current from a power source because power source, such as battery, inherently has two terminals of positive and negative terminals to complete a circuit loop.

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the Group customer service whose telephone number is 571-272-1626 and Fax number (703) 872-9306.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for this Group is (703) 872-9306.

hjt

6/5/2005

H. Jey Tsai
Primary Examiner
Patent Examining Group 2800